ABSTRACT OF THE DISCLOSURE

Conventionally, it is difficult to design the logic of a Gray code counter that can be used in interlaced counting. Even though interlaced counting is possible with a Gray code counter, the number of simultaneously changing bits increases greatly depending on the number of counts skipped at a time. To overcome these problems, a Gray code counter according to the present invention has a consecutively counting Gray code counter that counts in increments or decrements of one, and an output value converter circuit that converts the Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to decimal counts as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.